

Attorney's Docket No.: 10559-108001/P7613/Intel Corporation

Remarks

Reconsideration and allowance of this application are respectfully requested.

Claims 1, 3-8, 10-14, 16-20, 23 and 24 remain pending.

Claims 1, 8, 14, and 20 are in independent form.

CLAIMS 1 AND 20

In the action mailed October 20, 2003, claims 1 and 20 were rejected under 35 U.S.C. §103(a) as obvious over the admitted prior art (hereinafter "AAPA") and Perino et al. (U.S. Patent No. 6,160,716, hereinafter "Perino"). The rejections rely in part upon arguments presented in the Advisory Action mailed August 5, 2003.

These rejections are respectfully traversed. The rejections contend that it is appropriate to pick the limitation that the lines are connected to a single pin (from the AAPA) and combine this with the limitation that portions of the lines are parallel (from Perino).

It is respectfully suggested, however, that this combination is improper for at least the following reasons:

- 1) there is an **express teaching** in Perino stating that Perino's signal lines are not to be connected;
- 2) there are **express teachings** in Perino teaching away from a **non-grounded gap** between signal lines (which is an express claim limitation); and

Attorney's Docket No.: 10559-10800J/P7643/Intel Corporation

3) there is no suggestion to combine and/or a reasonable expectation of success founded in the prior art.

Applicant therefore respectfully submits that the proposed combination ignores the teachings of Perino as a whole and amounts to hindsight-based reconstruction of the claimed inventions.

To elaborate on 1) above, Perino expressly teaches away from contact between signal lines. Every signal line in Perino is routed around pins that are connected to another signal line. See, e.g., FIGS. 4, 7, 11, and 16 of Perino. Indeed, according to Perino, each signal line should not come close to, much less connect with, another signal line. "Closely spaced traces 130 may cause interference in some instances, or actual contact between the traces 130 if the traces are imperfectly fabricated." Perino, col. 2, lines 15-22. Indeed, the connection of Perino's parallel signal lines to a single pin will destroy the efficacy of Perino's device. One of ordinary skill who reads Perino would view the limitation that lines are connected as a manufacturing defect rather than a desirable result.

"A reference may be said to teach away when a person of ordinary skill, upon reading the reference, ... would be led in a direction divergent from the path that was taken by the applicant." *In re Gurley*, 27 F.3d 551 (Fed. Cir. 1994). The

Attorney's Docket No.: 10559-108001/P7643/Intel Corporation

totality of a reference's teachings must be considered when determining if a reference teaches away. W.L. Gore & Assoc., Inc. v. Garlock, Inc., 721 F.2d 1540, 1550-51 (Fed.Cir.1983), cert. denied, 469 U.S. 851 (1984). "As a 'useful general rule,' ... references that teach away cannot serve to create a *prima facie* case of obviousness." McGinley v. Franklin Sports, Inc., 262 F.3d 1339 (Fed. Cir. 2001).

Since, when considered in the entirety, Perino expressly teaches away from connecting signal lines to a single pin, it is respectfully submitted that Perino cannot serve to establish a *prima facie* case of obviousness.

To elaborate on 2) above, Perino further teaches away from another claim limitation, namely a non-grounded gap between signal lines. Attention is respectfully directed to FIG. 11 and the written description thereof, where Perino describes the advantages of ground traces 1160 intervening between signal lines 1170. "[G]round traces 1160 prevent interference." "[G]round traces 1160 reduce mutual capacitance and mutual inductance." "[B]y placing ground traces 1160 ... between the signal traces 1170, noise is reduced." Perino, col. 6, line 14-21.

In the action mailed October 20, 2003, it is contended that since the rejection does not rely upon FIG. 11 in rejecting the claims (and instead relies upon FIGS. 8 and 16), that Perino's

Attorney's Docket No.: 10559-108001/P7643/Intel Corporation

teaching regarding FIG. 11 are irrelevant to any proposed combination involving Perino. Applicant respectfully disagrees with this contention. To begin with, in discussing FIG. 11, Perino is contrasting Perino's invention of FIG. 11 with the prior art illustrated in FIG. 8, where there are no ground traces intervening between traces 870, 880. Perino's statements are thus express commentary on the embodiment shown in FIG. 8, which is the exact portion of Perino relied on in rejecting the claims.

In addition to this false premise, the law requires that the totality of a reference's teachings must be considered when determining if a reference teaches away, as discussed above. Simply put, a reference's teaching cannot be picked out of context and combined with another reference using the applicant's claims as a guide. Rather, the reference itself must suggest the combination to one of ordinary skill in the art.

To elaborate on 3) above, there is no suggestion to combine and reasonable expectation of success founded in the prior art. In the Advisory Action mailed August 5, 2003, it is contended that one of ordinary skill would be "motivated to employ the concept of the line width and space determination, as disclosed by Perino," to control the width and separation distance of

Attorney's Docket No.: 10559-108001/P7643/Intel Corporation

signal lines to eliminate reflected signals and signal deterioration.¹

However, Perino explicitly states that reflected signals and signal deterioration are caused by the structures in Perino relied on in rejecting the claims. "[T]wo-between routing' may cause interference between the signals carried by either of the traces." "[T]hin traces have an increased impedance, that does not match the impedance of the signals." Perino, col. 2, lines 15-33.

FIG. 8 explicitly illustrates two-between routing, as two traces 870, 880 are routed between two contact areas 850, 860. Thus, according to Perino, the embodiment of FIG. 8 relied upon in rejecting claims 1 and 20 is disadvantageous. The only teaching founded in Perino is that the proposed combination would be problematic.

It is therefore respectfully submitted that one of ordinary skill in the art would find no suggestion to combine Perino with the AAPA in the manner suggested. Accordingly, Applicant submits that claims 1 and 20, and the claims dependent therefrom, are allowable.

¹ "Eliminating reflected signals and signal deterioration caused by a mismatched impedance" is stated twice in the Advisory Action mailed August 5, 2003.

Attorney's Docket No.: 10559-108001/P7613/Intel Corporation

CLAIM 8

Independent claim 8 was rejected under 35 U.S.C. §103(a) as obvious over AAPA and Perino. This rejection is respectfully traversed.

Claim 8 relates to a method including delivering a first signal over a first signal line connected to a first pin on a memory unit and delivering a second signal over a second signal line connected to the first pin of the memory unit. A first portion of the second signal line is formed at an acute angle relative to a first portion of the first signal line. A second portion of the second signal line is formed substantially parallel to a second portion of the first signal line. The first and second portions of the first and second signal lines are separated without a ground connection therebetween.

As discussed above, the proposed combination ignores the teachings of Perino as a whole and amounts to hindsight-based reconstruction of the claims. Accordingly, Applicant submits that claim 8 and the claims dependent therefrom are allowable.

CLAIM 14

Independent claim 14 was rejected under 35 U.S.C. §103(a) as obvious over AAPA and Perino. This rejection is respectfully traversed.

Claim 14 relates to a method that includes connecting a memory unit to the board such that a first pin on the memory

Attorney's Docket No.: 10559-108001/P7643/Intel Corporation

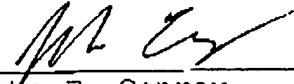
unit connects to first and second signal lines, forming a first portion of the second signal line to be at an acute angle relative to a first portion of the first signal line, and forming a second portion of the second signal line to be substantially parallel to a second portion of the first signal line.

As discussed above, the proposed combination ignores the teachings of Perino as a whole and amounts to hindsight-based reconstruction of the claims. Accordingly, Applicant submits that claim 14 and the claims dependent therefrom are allowable.

Applicant asks that all claims be allowed. Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 12/19/03


John F. Conroy
Reg. No. 45,485
Agent for: Intel Corporation

Fish & Richardson P.C.
PTO Customer Number: **20985**
12390 El Camino Real
San Diego, CA 92130
Telephone: (858) 678-5070
Facsimile: (858) 678-5099
10348964.doc